Aggregation Switch Deep Packet Inspection Hardware Offloading Benchmarks - Official Technical Overview & Hardware Datasheet

EXECUTIVE SUMMARY

The Aggregation Switch Deep Packet Inspection Hardware Offloading Benchmarks platform represents a paradigm shift in carrier-grade and enterprise aggregation layer design, specifically engineered to address the exponential growth of encrypted and application-specific traffic traversing modern backbone networks. Traditional Deep Packet Inspection (DPI) methodologies rely on software-based inspection engines that introduce significant latency, jitter, and throughput degradation when deployed at aggregation points exceeding 100 Gbps. This document details an OEM-grade hardware architecture that fundamentally resolves this bottleneck by embedding purpose-built DPI offloading silicon directly into the aggregation switch ASIC pipeline, delivering line-rate inspection at wire speed without compromising forwarding performance. The platform is optimized for service providers, large campus backbones, and datacenter leaf-spine fabrics requiring granular application visibility, policy enforcement, and security auditing at the aggregation tier. By offloading signature matching, flow state tracking, and heuristic analysis to dedicated hardware engines, the switch achieves sub-microsecond inspection latency while maintaining non-blocking throughput across all ports simultaneously. This datasheet provides

comprehensive benchmarks, architectural specifications, and deployment guidance for network architects evaluating hardware-accelerated DPI aggregation solutions.



HARDWARE ARCHITECTURE & SILICON

The core of the Aggregation Switch DPI Offloading platform is a custom multi-stage packet processing pipeline fabricated on a 7nm process node, integrating a high-density switching fabric with a dedicated DPI offload engine (DOE) cluster. Each DOE cluster comprises eight parallel signature-matching cores capable of executing regular expression and fixed-string matching against payloads at 400 Gbps aggregate throughput. The architecture employs a three-tier memory hierarchy: a 128 MB on-chip TCAM for active signature sets, a 4 GB HBM2e buffer for flow state and reassembly contexts, and an external

DDR5-4800 expansion slot for historical logging and forensic capture. The packet pipeline operates in a deterministic cut-through mode for known flows, while unknown or suspicious flows are steered to the DOE cluster for deep inspection without interrupting the forwarding path. Hardware offloading is transparent to control-plane protocols, with DPI policies provisioned via NETCONF/YANG or OpenFlow 1.5 extensions. The switching fabric itself delivers 12.8 Tbps non-blocking capacity across 32x400GE or 64x200GE line card configurations, with a shared packet buffer of 64 MB dynamically allocated across all ports to absorb microbursts during inspection-intensive workloads.

KEY FEATURES & ROUTING LOGIC

- Hardware DPI Offload Engine: Eight-core signature matching cluster delivering 400 Gbps inspection throughput with sub-microsecond added latency, supporting 50,000+ concurrent signature rules.
- Line-Rate Forwarding with Inspection: Non-blocking 12.8 Tbps switching capacity maintained during active DPI processing, eliminating the throughput penalty associated with software-based inspection.
- Flow State Aware Processing: Hardware-managed flow tables track 4 million concurrent flows with automatic TCP reassembly, TLS metadata extraction, and application identification for 3,500+ protocols.
- Policy-Based Forwarding Integration: DPI verdicts directly influence routing

decisions via hardware ACLs and PBR (Policy-Based Routing) tables, enabling application-aware traffic engineering.

- Encrypted Traffic Metadata Analysis: Hardware extraction of SNI, JA3/JA3S fingerprints, and certificate metadata from TLS 1.3 handshakes without decryption, preserving privacy while enabling classification.

- Redundant DPI Engine Failover: Dual DOE clusters operating in active-active mode with hitless failover, ensuring inspection continuity during component failure.

- Streaming Telemetry Export: Hardware-accelerated IPFIX and gRPC telemetry streams export DPI verdicts, flow statistics, and signature hit counters at 1-second granularity.

COMPLIANCE & STANDARDS

The platform complies with major international telecom and networking standards, ensuring interoperability and regulatory adherence across global deployments. Electromagnetic compatibility is certified to FCC Part 15 Subpart B Class A, EN 55032 Class A, and VCCI Class A. Safety certifications include UL 62368-1, IEC 62368-1, and EN 62368-1 for operator and service personnel protection. Environmental compliance encompasses RoHS 2011/65/EU, WEEE 2012/19/EU, and REACH Article 33. Network protocol compliance includes IEEE 802.1Q, 802.1ad, 802.1ah, 802.3ba, 802.3bs, and 802.3cd for Ethernet framing

and link aggregation. Routing and switching standards supported comprise RFC 1812 (IPv4 routers), RFC 8200 (IPv6), RFC 4271 (BGP-4), RFC 5308 (IS-IS), RFC 2328 (OSPFv2), and RFC 5340 (OSPFv3). DPI-specific compliance includes ETSI GS ISI 001 for lawful interception interfaces (where jurisdictionally applicable) and 3GPP TS 33.107 for policy and charging enforcement function integration. MEF 3.0 certification ensures Carrier Ethernet service delivery with DPI-enhanced CoS mapping.

TECHNICAL SPECIFICATIONS

Parameter	Specification
Form Factor	1RU Standard / 2RU Modular Chassis (model dependent)
Switching Capacity	12.8 Tbps non-blocking full-duplex
DPI Offload Throughput	400 Gbps aggregate inspection bandwidth
Inspection Latency	< 1 microsecond added per packet at line rate
Concurrent Flows	4,000,000 hardware-tracked flow entries
Signature Capacity	50,000 concurrent rules across active policy set

Packet Buffer	64 MB shared across all ports
Power Supply	Dual Hot-Swappable Redundant AC/DC (model dependent)
Airflow	Front-to-Back or Reverse (model dependent)
Operating Temperature	0°C to 45°C (32°F to 113°F)
Management Interfaces	1x RJ45 Console, 1x 10/100/1000BASE-T Mgmt, 1x USB 3.0
Telemetry Export	IPFIX, gRPC, sFlow v5
Compliance	FCC, CE, UL, RoHS, WEEE, MEF 3.0
MTBF	> 250,000 hours (Telcordia SR-332 Issue 3)

ORDERING SKU INFORMATION

The Aggregation Switch DPI Offloading platform is available in three base configurations to suit varying deployment scales and redundancy requirements. The AS-DPI-32P-AC model provides 32x400GE QSFP-DD ports with dual hot-swappable AC power supplies and front-to-back airflow. The AS-DPI-64P-DC variant offers 64x200GE QSFP56 ports with dual DC power feeds and reverse airflow for telecom central office environments. The

AS-DPI-16P-HYB is a hybrid configuration featuring 16x400GE and 32x100GE ports with mixed AC/DC power options and field-replaceable fan trays. All models include the integrated DPI offload engine cluster as standard; no separate licensing or hardware module is required for base inspection functionality. Advanced signature packs, historical forensic capture licenses, and extended telemetry retention are available as software add-ons via the OEM licensing portal. Spare components including power supplies, fan trays, and transceiver cages are orderable as field-replaceable units (FRUs) with individual SKUs for simplified sparing logistics.

